Reg. No: ☐☐☐☐☐☐☐☐☐☐☐☐

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech I Year II Semester Supplementary Examinations July-2021
DIGITAL LOGIC DESIGN
(Common to CSE & CSIT)

Time: 3 hours   Max. Marks: 60

PART-A
(Answer all the Questions **5 x 2 = 10** Marks)

1	a	Which gates are called as the universal gates? What are its advantages?	2M
	b	What are called don't care conditions?	2M
	c	Write any two differences between encoder and decoder.	2M
	d	What is state diagram?	2M
	e	List the major differences between PLA and PAL.	2M

PART-B
(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2   a   Determine the value of base x if$(211)x=(152)_8$ 5M
    b   Explain the Excess-3 code? Write about Error correction & Detection.   5M

OR

3   a   State and Explain the DeMorgan's Theorem and Consensus Theorem.   5M
    b   Explain the Binary codes with examples.   5M

UNIT-II

4   Simplify the Boolean expression using K-MAP   10M
    $F(A,B,C,D) = \sum m(1,2,3,8,9,10,11,14) + d(7,15)$.

OR

5   Simplify the Boolean expression using K-map.   10M
    $F(A,B,C,D,E) = \sum m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$.

UNIT-III

6   a   Implement the following Boolean function using 8:1 multiplexer.   5M
      $F(A,B,C.D) = \sum m (0,1,2,5,7,8,9,14,15)$
    b   Explain about Binary Multiplier.   5M

OR

7   a   Design the combinational circuit of 4 Bit Parallel Adder.   5M
    b   Explain full binary subtractor in detail.   5M

UNIT-IV

8   a   Draw and explain the operation of SR LATCH.   5M
    b   Explain about Ring counter.   5M

OR

9   Design 4-bit binary synchronous counter with D-flip flop.   10M

UNIT-V

10   Construct the PROM using the conversion from BCD code to Excess-3 code.   10M

OR

11   a   Explain about TTL family.   5M
    b   Explain about CMOS Logic.   5M

END